

**Preliminary Amendment filed February 22, 2005
U.S. Patent Application Serial No. 10/634,839**

REMARKS:

Claims 1-5 are currently being considered, of which claim 1 has been amended. Claim 6 has been canceled without prejudice or disclaimer of its subject matter. No new claims have been added. No new matter has been introduced.

Before turning to the cited references, a brief review of the present invention is in order. The present invention relates to a method for manufacturing a semiconductor device, comprising the steps of: (a) forming a laminated substrate by laminating a device formation layer consisting of single crystalline semiconductor on a supporting substrate consisting of single crystalline semiconductor via an insulating layer wherein a direction of a crystallographic axis of the device formation layer is shifted from a corresponding crystallographic axis of the supporting substrate; (b) forming semiconductor devices on the device formation layer within a plurality of areas divided by scribe lines, the scribe lines extending to a direction being parallel to a direction of a crystallographic axis of the supporting substrate where the supporting substrate is easy to be cleaved; and (c) splitting the laminated substrate into a plurality of chips by cleaving the supporting substrate along the scribe lines.

The scribe lines are defined on the device formation layer and are not defined on the supporting substrate. According to the principles of the present invention, a wiring layer is formed comprising wiring wherein at least 70% of a full length of all the wiring in the wiring

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layer extends to a direction being substantially parallel to a direction of a crystallographic axis of the supporting substrate.

Claims 1-6 stand rejected under 35 USC 103(a) as obvious over JP 09-246505 (**Kato**), USP 3,054,709 (**Freestone**), and USP 6,596,185 (**Lin**).

Applicants respectfully traverse this rejection.

Freestone, Kato, and Lin, alone or in combination, fail to describe, teach or suggest the following features of claim 1, as amended: “(b) forming semiconductor devices on the device formation layer within a plurality of areas divided by scribe lines, the scribe lines being defined on the device formation layer and not on the supporting substrate, the scribe lines extending to a direction being parallel to a direction of a crystallographic axis of the supporting substrate where the supporting substrate is easy to be cleaved; and (c) splitting the laminated substrate into a plurality of chips by cleaving the supporting substrate along the scribe lines; wherein the step (b) further comprises the step of forming a wiring layer comprising wiring wherein at least 70% of a full length of all the wiring in the wiring layer extends to a direction being substantially parallel to a direction of a crystallographic axis of the supporting substrate where the supporting substrate is easy to be cleaved”, in combination with the other claimed features.

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Thus, Applicants respectfully submit that this rejection should be withdrawn.

In view of the aforementioned remarks, all claims currently being considered are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

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